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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,680	06/30/2000	Brad A. Barnore	042390.P8527	1233

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EXAMINER

CASIANO, ANGEL L

ART UNIT	PAPER NUMBER
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2182

DATE MAILED: 04/21/2004

12

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/607,680

Applicant(s)

BARMORE, BRAD A.

Examiner

Angel L. Casiano

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The present Office action is in response to amendment dated 05 February 2004.
2. Claims 1-27 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pecone [US 5,604,871] in view of Maleck et al. [US 6,611,912 B1].

Regarding Claim 1, Pecone discloses a system including a motherboard (col. 2, lines 49-50) coupled to data, address, control, power and ground signals, as well as a riser card having interface and logic circuits (col. 2, lines 53-54). Although the reference does not explicitly mention a chipset, it would have been obvious to one of ordinary skill in the art that the term "chipset" referred to integrated circuits designed to perform one or more

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functions. The reference also discloses a memory, intended to store a sequence of instructions, coupled with the motherboard (col. 3, lines 33-35). Accordingly, Pecone also teaches a riser card coupled with the motherboard (col. 7, lines 1-4; lines 34-38), having a circuit (col. 4, line 67; col. 5, lines 2-5; col. 3, line 35) that interacts with a portion of the integrated circuits ("chipset") to provide a functionality (col. 3, line 37) and having a memory (col. 3, line 34) to store one or more indications of the functionality. Pecone does not include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. In addition, Pecone does not expressly disclose the riser card operating as a logical extension of the motherboard. Furthermore, Pecone fails to provide an external interface for the motherboard. Maleck et al. teaches a riser card operating as an extension of the motherboard (see Abstract). In addition, Maleck et al. teaches a memory (see "storage device") for storing a sequence of instructions (see Abstract). In addition, Maleck et al. teaches loading a driver, as part of the system (see col. 4, lines 7-9; Figure 1, system 100, riser card 106). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited art in order to provide plug and play (PnP) functionality. Moreover, it is well known in the art that a "driver" refers to code that works to communicate an operating system and a peripheral. Furthermore, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a system having autonomous configuration of devices coupled to a data processing system (see Maleck et al., col. 1, lines 10-12).

As for Claim 2, the Pecone reference includes a riser card coupled with the motherboard via a slot interface having pins (see col. 8, lines 13-17; col. 7, lines 34-38) corresponding to one or more predetermined standards (see col. 3, lines 1-3).

As for Claim 3, Pecone does not specify the memory of the riser card as ROM. A BIOS boot sequence is not disclosed by the cited art. However, Maleck et al. teaches a system, having a riser card, Basic Input/Output Software (BIOS) and a Read-Only Memory (see "EEPROM", col. 2, line 40).

As for Claims 4-8, the claimed functionalities constitute specific examples of the possible applications of the system disclosed by the combination of references and exposed in claim 1. Therefore, these claims are rejected under the same rationale.

As for Claim 9, Pecone fails to include a sequence of instructions to cause a driver to be loaded. Maleck et al. teaches a riser card operating as an extension of the motherboard (see Abstract). In addition, Maleck et al. teaches a memory (see "storage device") for storing a sequence of instructions (see Abstract). In addition, Maleck et al. teaches loading a driver, as part of the system (see col. 4, lines 7-9; Figure 1, system 100, riser card 106). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited prior art in order to provide plug and play (PnP) functionality.

Regarding Claim 10, Pecone teaches a system including a motherboard (col. 2, lines 49-50) and a riser card having an interface and logic circuits (col. 2, lines 53-54). Although the reference does not explicitly mention a coupled “chipset”, it would have been obvious to one of ordinary skill in the art that the term “chipset” implied integrated circuits designed to perform one or more functions. This term is commonly used in reference to the core functionality of a motherboard. The reference discloses a memory, intended to store a sequence of instructions, coupled with the motherboard (col. 3, lines 33-35). In addition, Pecone teaches a riser card coupled with a motherboard (col. 7, lines 1-4; lines 34-38), having a circuit (col. 4, line 67; col. 5, lines 2-5; col. 3, line 35) that interacts with a portion of the integrated circuits (see “chipset”) to provide a functionality (col. 3, line 37) and also having a memory (col. 3, line 32) to store one or more indications of the functionality. Pecone does not include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. Maleck et al. teaches a riser card operating as an extension of the motherboard (see Abstract). In addition, Maleck et al. teaches a memory (see “storage device”) for storing a sequence of instructions (see Abstract). In addition, Maleck et al. teaches loading a driver, as part of the system (see col. 4, lines 7-9; Figure 1, system 100, riser card 106). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited references in order to provide plug and play (PnP) functionality. It is well known in the art that a driver is a code that works to communicate an operating system and a peripheral.

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As for Claim 11, the Pecone reference teaches a riser card coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined standards (see col. 8, lines 13-17; col. 7, lines 34-38; col. 3, lines 1-3; col. 5, lines 6-7).

As for Claim 12, Pecone does not specify the memory of the riser card as ROM. A BIOS boot sequence is not disclosed by the cited art. However, Maleck et al. teaches a system, having a riser card, Basic Input/Output Software (BIOS) and a Read-Only Memory (see "EEPROM", col. 2, line 40).

As for Claims 13-17, these limitations (audio codec, modem codec, USB support, SMBus device support, and networking functionality) constitute specific examples of the possible applications for the riser card disclosed by the combination of references, as exposed previously. Therefore, these claims are rejected under the same rationale.

As for Claim 18, Pecone does not explicitly disclose a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. Maleck et al. teaches a riser card operating as an extension of the motherboard (see Abstract). In addition, Maleck et al. teaches a memory (see "storage device") for storing a sequence of instructions (see Abstract). In addition, Maleck et al. teaches loading a driver, as part of the system (see col. 4, lines 7-9; Figure 1, system 100, riser card 106). The cited driver is loaded by an operating system (see col. 6, lines 16-19, 60-62).

Regarding Claim 19, the reference discloses a memory, for storing a sequence of instructions, coupled with the motherboard (col. 3, lines 33-35), as claimed. The reference also discloses a system comprising a motherboard (col. 2, lines 49-50) coupled to data, address, control, power and ground signals, as well as a riser card having an interface and logic circuits (col. 2, lines 53-54). Although the reference does not explicitly mention a “chipset”, as it is well known in the art, the term “chipset” refers to integrated circuits designed to perform one or more functions. This term is commonly used in reference to the core functionality of the motherboard. In another aspect of the claim, Pecone does not expressly disclose the riser card operating as a logical extension of the motherboard. Pecone does not expose providing an external interface for the motherboard. Maleck et al. teaches a riser card operating as an extension of the motherboard (see Abstract). In addition, Maleck et al. teaches a memory (see “storage device”) for storing a sequence of instructions (see Abstract). In addition, Maleck et al. teaches loading a driver, as part of the system (see col. 4, lines 7-9; Figure 1, system 100, riser card 106). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited art in order to provide plug and play (PnP) functionality. Moreover, it is well known in the art that a “driver” refers to code that works to communicate an operating system and a peripheral. Furthermore, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a system having autonomous configuration of devices coupled to a data processing system (see Maleck et al., col. 1, lines 10-12).

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As for Claim 20, Pecone includes a riser card coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined standards (see col. 8, lines 13-17; col. 7, lines 34-38; col. 3, lines 1-3), as claimed.

As per Claim 21, Pecone does not specify the memory of the riser card as ROM. A BIOS boot sequence is not disclosed by the cited art. However, Maleck et al. teaches a system, having a riser card, Basic Input/Output Software (BIOS) and a Read-Only Memory (see "EEPROM", col. 2, line 40).

As for Claims 22-26, the claimed limitations (audio codec, modem codec, USB support, SMBus device support, and networking functionality) constitute specific examples of possible applications of the memory disclosed by the combination of references, as exposed previously. Therefore, these claims are rejected under the same rationale.

As for Claim 27, Pecone does not explicitly disclose a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. Maleck et al. teaches a riser card operating as an extension of the motherboard (see Abstract). In addition, Maleck et al. teaches a memory (see "storage device") for storing a sequence of instructions (see Abstract). In addition, Maleck et al. teaches loading a driver, as part of the system (see col. 4, lines 7-9; Figure 1, system 100, riser card 106). The cited driver is loaded by an operating system (see col. 6, lines 16-19, 60-62).

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Response to Arguments

5. Applicant's arguments, see Amendment, filed 05 February 2004, with respect to the Rejection of claims 1-27 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Maleck et al. [US 6,611,912 B1].

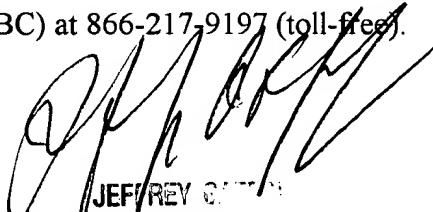
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 703-305-8301. The examiner can normally be reached on 9:30-6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217,9197 (toll-free).

alc
15 April 2004.


JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
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